Fermilab

PMC-DAS1 Serial Link

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Link Characteristics

PMC-to-DARC (Data Acq. Remote Chassis) Link

- 160 or 320 Mbps using Cypress Hotlink chipset (cable selectable, readable from link status register)
- Transformer coupled
- Five byte transmission packet with four byte payload
- Transmission sequence: PKT-FRM, LSB0 (D7-D0), LSB1 (D15-D8), MSB0 (A7-A0), MSB1 (CTL3-CTL0, A11-A8)
- DARC packets are framed with K28.0 Special Character, (Future application) packets are framed with K28.7 Special Character
- Byte framing maintained by K28.5 Sync when link is idle

DARC-to-PMC Link

- 160 or 320 Mbps using Cypress Hotlink chipset (cable selectable)
- Transformer coupled
- Five byte transmission packet with four byte payload
- Transmission sequence: PKT-FRM, LSB0 (D7-D0), LSB1(D15-D8), MSB0(A7-A0), MSB1(TC3-TC0,A11-A8)
- Packet is framed with K28.0 Special Character
- Byte framing maintained by K28.5 Sync when link is idle
- No link maintenance feedback from PMC to DARC
- PMC maintains running counts of various types of transmission errors. Counters stop at ceiling value until reset by the system processor.

Data Types

Slow Data Timestamp

- From remote chassis
- Precedes slow data block
- MSW followed immediately by LSW in two back-to-back packets
- 16 bit value, type code, MSW/LSW flag
- Internal S-D block counter is used as index to store timestamp
- Acquire complete timestamp, increment block counter, and store data to RAM

31 28	27 17	16	15 0
Type_Code=6	0000 0000 000	MSW Flag=1	MS Timestamp

31 28	27 17	16	15 0
Type_Code=6	0000 0000 000	LSW Flag=0	LS Timestamp

Slow Data

- From remote chassis
- Single packet
- 10 Khz fixed repetition rate
- 64 channels
- 16 bit conversion value, channel nr., type code
- Channel nr. combined with internal S-D block count is used as index into memory buffer
- Store data to RAM using block count and channel number as index

31 28	27 22	21 16	15 0
Type_Code=0	0000 00	Channel Nr	Data

Snapshot Timestamp

- From remote chassis
- Precedes snapshot data
- MSW followed immediately by LSW in two back-to-back packets
- 16 bit value, type code, MSW/LSW flag
- Placed into next available location in snapshot buffer memory
- Store data to fixed RAM address, reset snapshot address counter

31 28	27 17	16	15 0
Type_Code=5	0000 0000 000	MSW Flag=1	MS Timestamp

31 28	27 17	16	15 0
Type_Code=5	0000 0000 000	LSW Flag=0	LS Timestamp

Snapshot Data

- From remote chassis
- Up to 10 Msamples/sec burst, captured at remote chassis
- Maximum of 16 Ksamples on 8 channels per trigger
- 16 bit conversion value, channel nr., type code
- Placed sequentially into snapshot buffer after timestamp using local address counter. Address is reset upon receipt of Snapshot LS Timestamp. Address counter is incremented after receipt and store of channel nr.7 data. Thus, if one sample is lost, subsequent sample sets will not be skewed in memory (which could occur if a counter-per-channel is used).
- Store data to RAM using current snapshot address counter value

31 28	27 19	18 16	15 0
Type_Code=4	0000 0000 0	Channel Nr.	Data

Fast Data Timestamp

- From remote chassis
- Precedes fast data
- MSW followed immediately by LSW in two back-to-back packets
- 16 bit value, type code, MSW/LSW flag
- Internal F-D block counter is used as index into fast data buffer
- Acquire complete timestamp, increment block counter, and store data to RAM

31 28	27 17	16	15 0
Type_Code=7	0000 0000 000	MSW Flag=1	MS Timestamp

31 28	27 17	16	15 0
Type_Code=7	0000 0000 000	LSW Flag=0	LS Timestamp

Fast Data

- From remote chassis
- Single packet
- 100 Khz fixed repetition rate
- 64 channels
- 16 bit conversion value, channel nr., type code
- Channel nr. combined with internal F-D block count is used as index into memory buffer
- Store to RAM

31 28	27 22	21 16	15 0
Type_Code=1	0000 00	Channel Nr	Data

Digital Input/Digital Output Readback/Status/Control Register Readback

- From remote chassis
- Single packet
- Periodically updated by remote chassis
- 16 bit data, type code, 12 bit register address
- Cached in local memory

31 28	27 16	15 0
Type_Code= b11xx	Register Address	Data

TC = F, b1111: both bytes written
TC = E, b1110: high byte only
TC = D, b1101: low byte only
TC = C, b1100: neither byte

Remote Unit Interrupt

- From remote chassis
- Single packet
- Raises LINT1 to the PLX9050.
- LINT1 can be programmed via the INTCSR (PLX local register 4C) to trigger a PCI interrupt
- Interrupt status can be read and cleared at PMC local register 0x50 000E

31 28	27 16	15 0
Type_Code= B	0	0

Control/Output Register Update

- To remote chassis
- Dump-'n-run from PCI bus
- Single word, flag always zero
- R/W bit=0, 2 byte enables, spare bit=0, 12 bit register address, 16 data
- No memory operation

31	30	29	28	27 16	15 0
RW 0	BHE	BLE	SPARE 0	ADR	D15 D0

(Undefined) Operation

- To remote chassis
- Unique packet framing character

- 32 bits undefined (possible firmware download?)
- Initial implementation to be PCI write, dump-'n-run
- Can use open type codes for return data from remote chassis

PMC Local Registers

- No remote chassis transaction is generated by a local status read/write

50 0000 & R – Slow Data Block Count

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 0002 & R – Fast Data Block Count

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 0004 & R – Snapshot Address

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 0006 & R – Received Violation Symbol Count

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 0008 & R – Received Packet Error Count

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 000A & R – Receiver Test Loop Count

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 000C & R – Transmitter Test Loop Count

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

50 000E & R – Link Status

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	link test	irq	slow	snap done	x	x	x	x	x	x	x	x	x	rx ovrn

rx ovrn – receiver overrun
slow – link speed is 160 Mbps when set
snap done – snapshot address counter is at terminal count
irq – a typecode B packet was received from the remote unit indicating an interrupt event occurred.

50 000E & W – Reset Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	link test	x	x	x	rst irq	rst sna	rst fbc	rst sbc	rst link	rst txct	rst rxct	rst pker	rst rxerr	rst ovrn

Rst ovrn – Write “1” to reset the receiver overrun flag
Rst rxerr – Write “1” to reset the received violation symbol error counter
Rst pker – Write “1” to reset the received packet error counter
Rst rxct – Write “1” to reset the receiver test loop counter
Rst txct – Write “1” to reset the transmitter test loop counter
Rst link – Write “1” to reset the link
Rst sbc – Write “1” to reset the slow data block counter
Rst fbc – Write “1” to reset the fast data block counter
Rst sna – Write “1” to reset the snapshot address counter
Rst irq – Write “1” to reset the remote unit interrupt status
Tx tst – Places Hot-link transmitter into test mode
Rx tst – Places Hot-link receiver into test mode
Loopback – Loops Hot-link transmitter into the receiver

Local Memory Organization

SPACE	TC	Range	22 20	19 16	15 12	11 8	7 4	3 0
Slow Data	0	00 0000-1F FFFF	00B	BBBB	BBBB	BBBB	BNNN	NNNA
Fast Data	1	20 0000-3F FFFF	01B	BBBB	BBBB	BBBB	BNNN	NNNA
Snapshot Data	4	40 0000-43 FFFF	100	00NN	NSSS	SSSS	SSSS	SSSA
Snapshot Data Timestamp	5	45 FFFC-45 FFFF	100	0101	1111	1111	1111	11AA
Slow Data Timestamp	6	46 0000-46 FFFF	100	0110	BBBB	BBBB	BBBB	BBAA
Fast Data Timestamp	7	47 0000-47 FFFF	100	0111	BBBB	BBBB	BBBB	BBAA

Error Count and Status Registers	x	50 0000-5F FFFF	101	XXXX	XXXX	XXXX	XXXX	RRRA
Remote Register Cache	C-F	48 0000-48 1FFF	100	1000	000R	RRRR	RRRR	RRRA

One block of 2Mx16, one block of 512Kx16

Revision History

10 Oct 02
Merged typecodes for Digital Input Read, D, and Digital Output Register Readback, F, into typecode E. Changed typecode for Control/Status Register Readback to F from E. Uncommitted typecodes are 2,3,8,9,A,B,C, and D.

10 Jun 03
Changed bit definitions of 0x50000E status/control register

20 Nov 03
Added byte enables to register updates by redefining typecodes C through F

1 Nov 05
Added Typecode B interrupt to PCI. Removed CSR cache dirty/clean flag at 50000E. Added interrupt status and interrupt reset at 50000E.